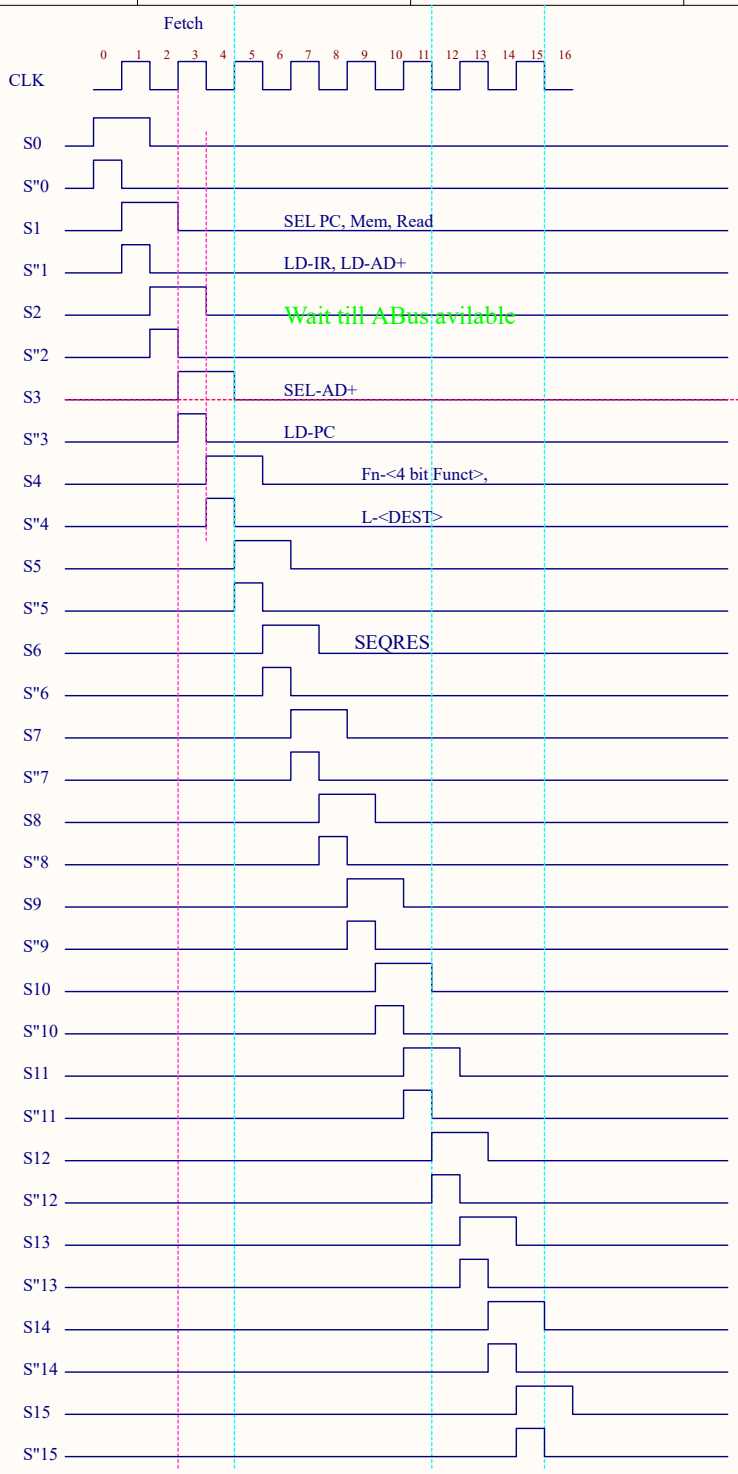
ALU

Sixteen stage state machine



MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

ALU

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

ALU Fn

0000 = NOP
0001= RESET
0010 = HALT
0011= WAIT0
1000 = ADDAB
1001 = A&B
1010 = NOTA
1011 = INCB
1100 = RORA
1101 = ROLB

DES

A=00
B=01
C=02

Proposed Update 1/1/20

BRANCH

2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-ALU.SchDoc		Drawn By:

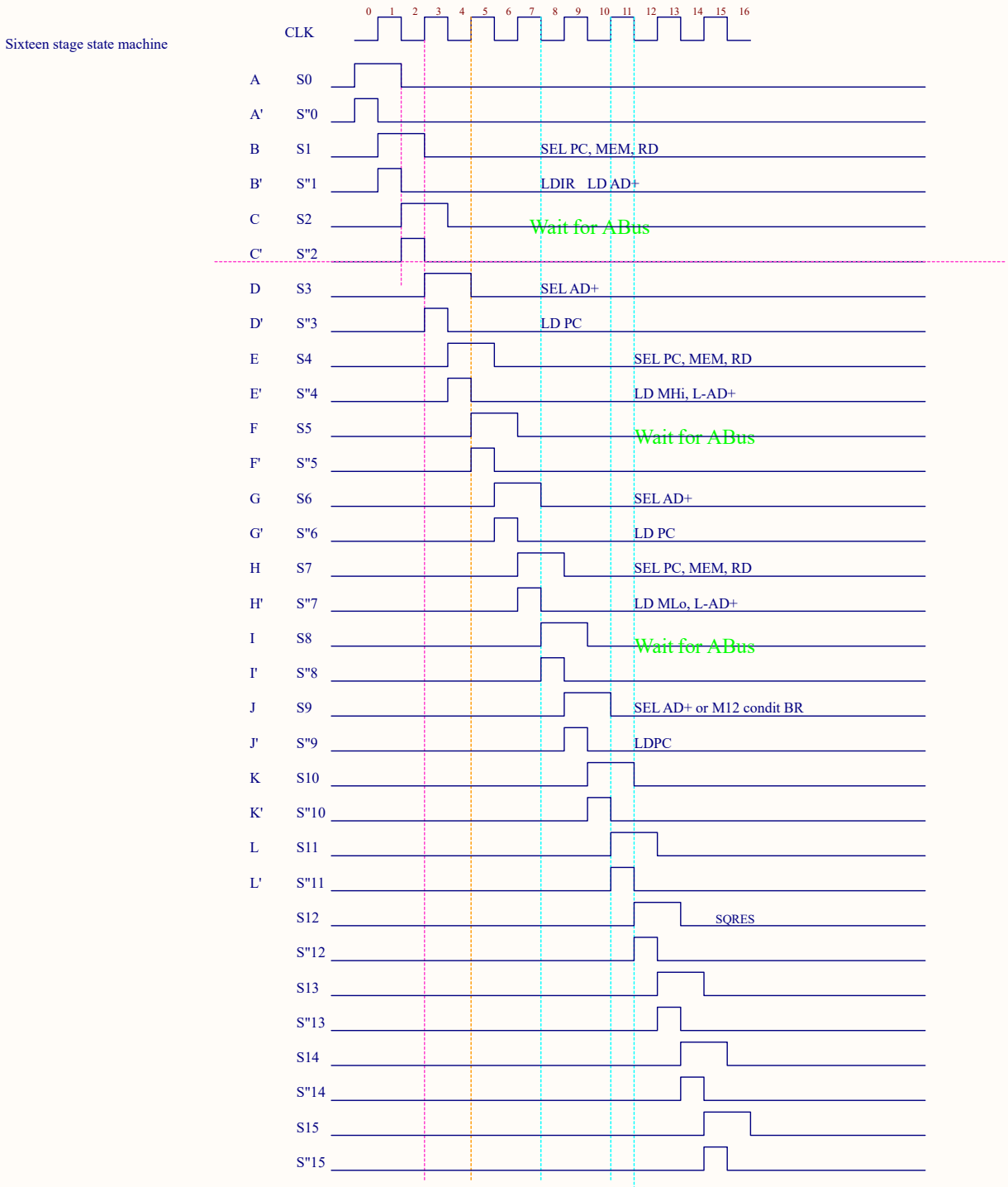
BRA

BRA

BRA

Fetch

Sixteen stage state machine



BRA

2/4/2

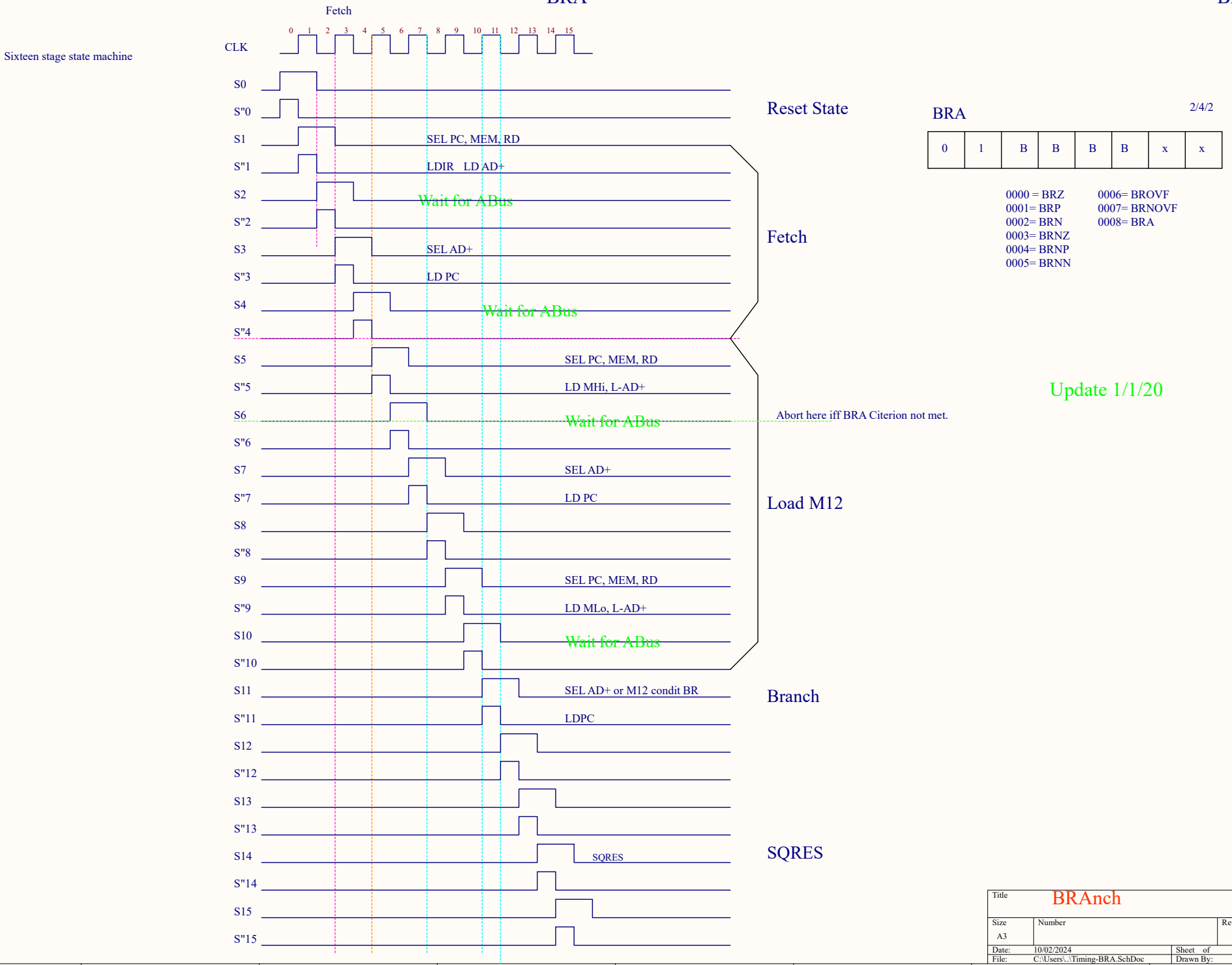
0	1	B	B	B	B	x	x

0000 = BRZ
0001= BRP
0002= BRN
0003= BRNZ
0004= BRNP
0005= BRNN
0006= BROVF
0007= BRNOVF
0008= BRA

Proposed Update 1/1/20

Title: BRAnch		
Size: A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\TimingBRA.SchDoc		Drawn By:

BRA BRA BRA



BRA 2/4/2

0	1	B	B	B	B	x	x

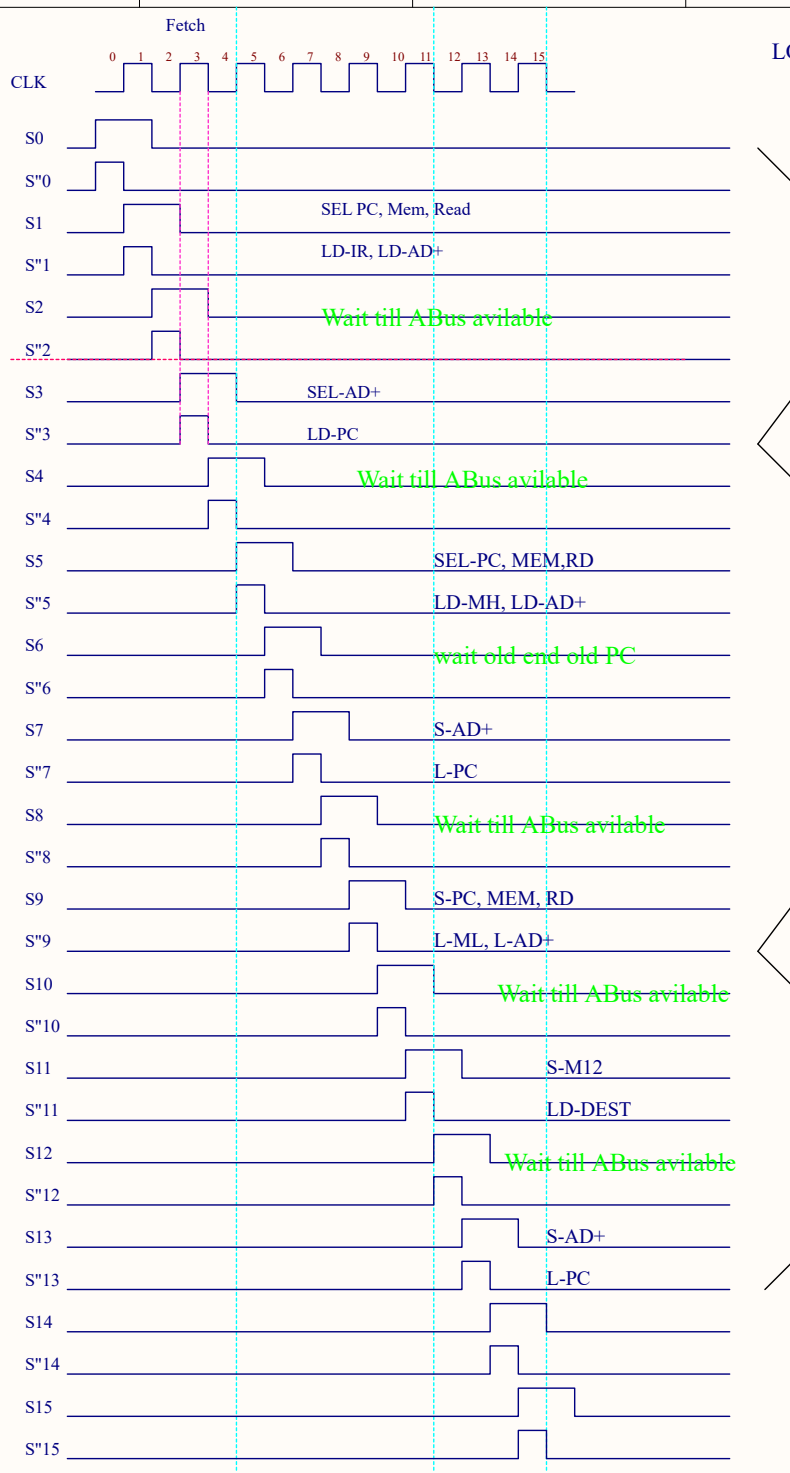
0000 = BRZ
0001= BRP
0002= BRN
0003= BRNZ
0004= BRNP
0005= BRNN
0006= BROVF
0007= BRNOVF
0008= BRA

Update 1/1/20

Title: BRAnch		
Size: A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-BRA.SchDoc		Drawn By:

LDA<REG>

Sixteen stage state machine



LOAD REG from MEM ABSOLUTE

LDA<REG>

MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

SRC	DEST	Temp
000 = A	000 = A	000 = A
001 = B	001 = B	100 = B
010 = C	010 = C	001 = C
011 = MMI	011 = nul	
100 = MMA	100 = MMA	010 = MMA
111 = nul		

NB If DEST is MMA, then must be RAM
If SRC is MMI (Immediate) then can be ROM or RAM
If SRC is MMA (Absolute), can be ROM or RAM

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

Fetch

Proposed Update 1/1/20

Load M12

BRANCH

2/4/2 instructions

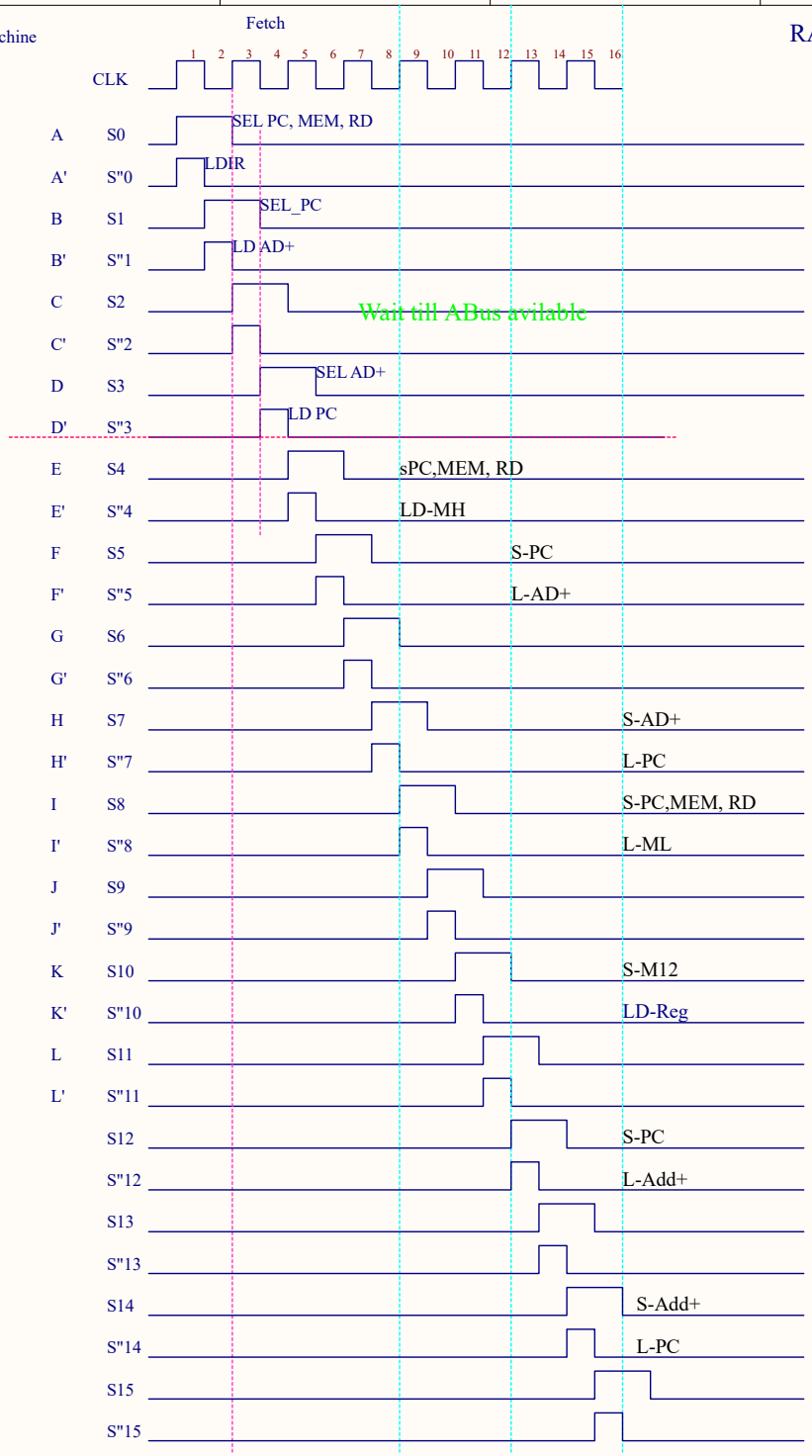
IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

Load REG from MEM

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-LDA(Read).SchDoc		Drawn By:

Sixteen stage state machine

RAM Read



MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S R	S	S	D W	D	D

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
2	2	S	S	S	D	D	D

BRANCH

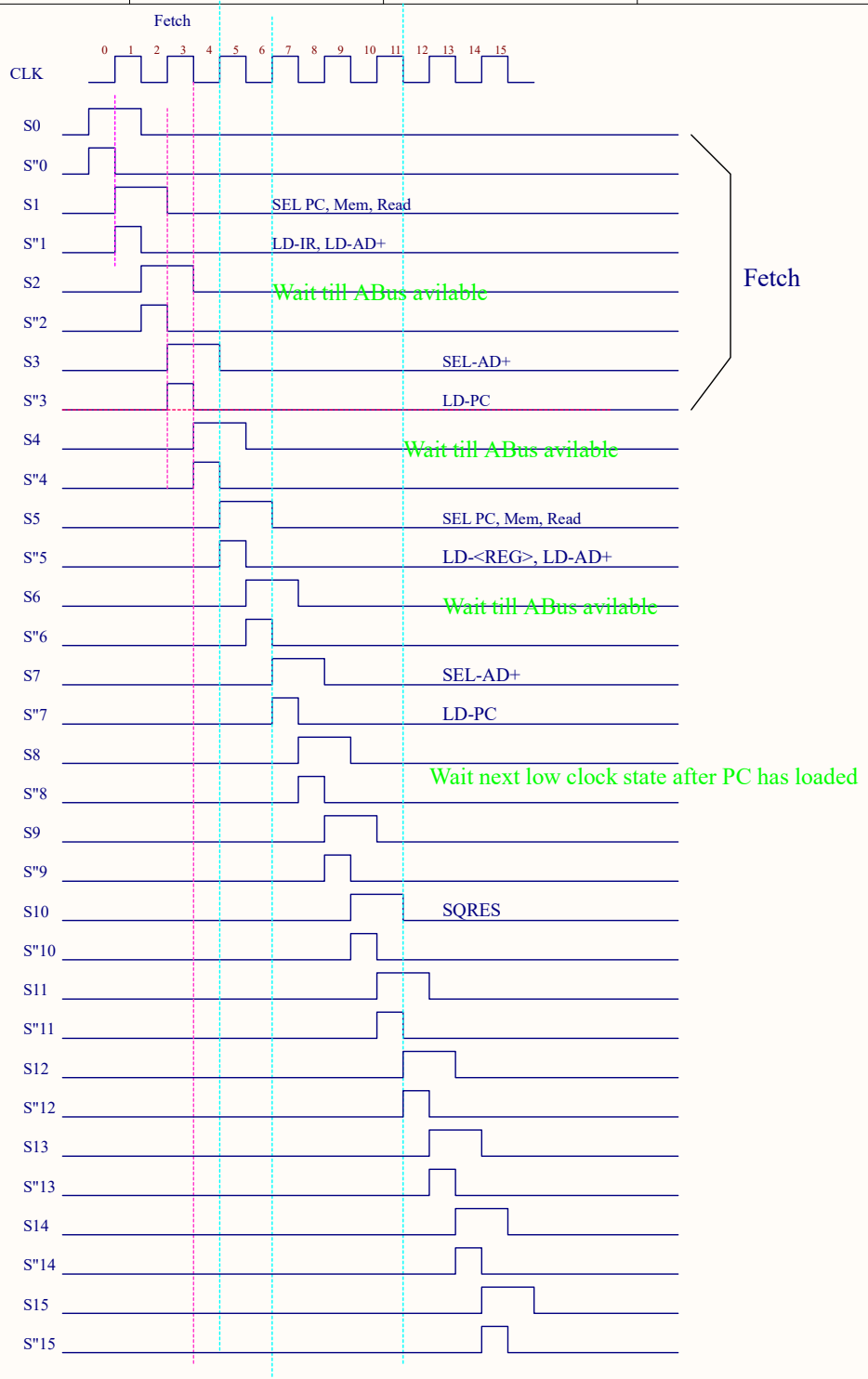
2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

Title	RAM write	
Size: A3	Number	Revision
Date: 10/02/2024	Sheet of	
File: C:\Users\..\Timing-LDAA(Read).SchDoc	Drawn By:	

LDI<reg>

Sixteen stage state machine



Fetch

MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

SRC	DEST	Temp
000 = A	000 = A	000 = A
001 = B	001 = B	100 = B
010 = C	010 = C	001 = C
011 = MMI	011 = nul	
100 = MMA	100 = MMA	010 = MMA

NB If DEST is MMA, then must be RAM
If SRC is MMI (Immediate) then can be ROM or RAM
If SRC is MMA (Absolute), can be ROM or RAM

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

LDI<reg>

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

Update 1/1/20

BRANCH

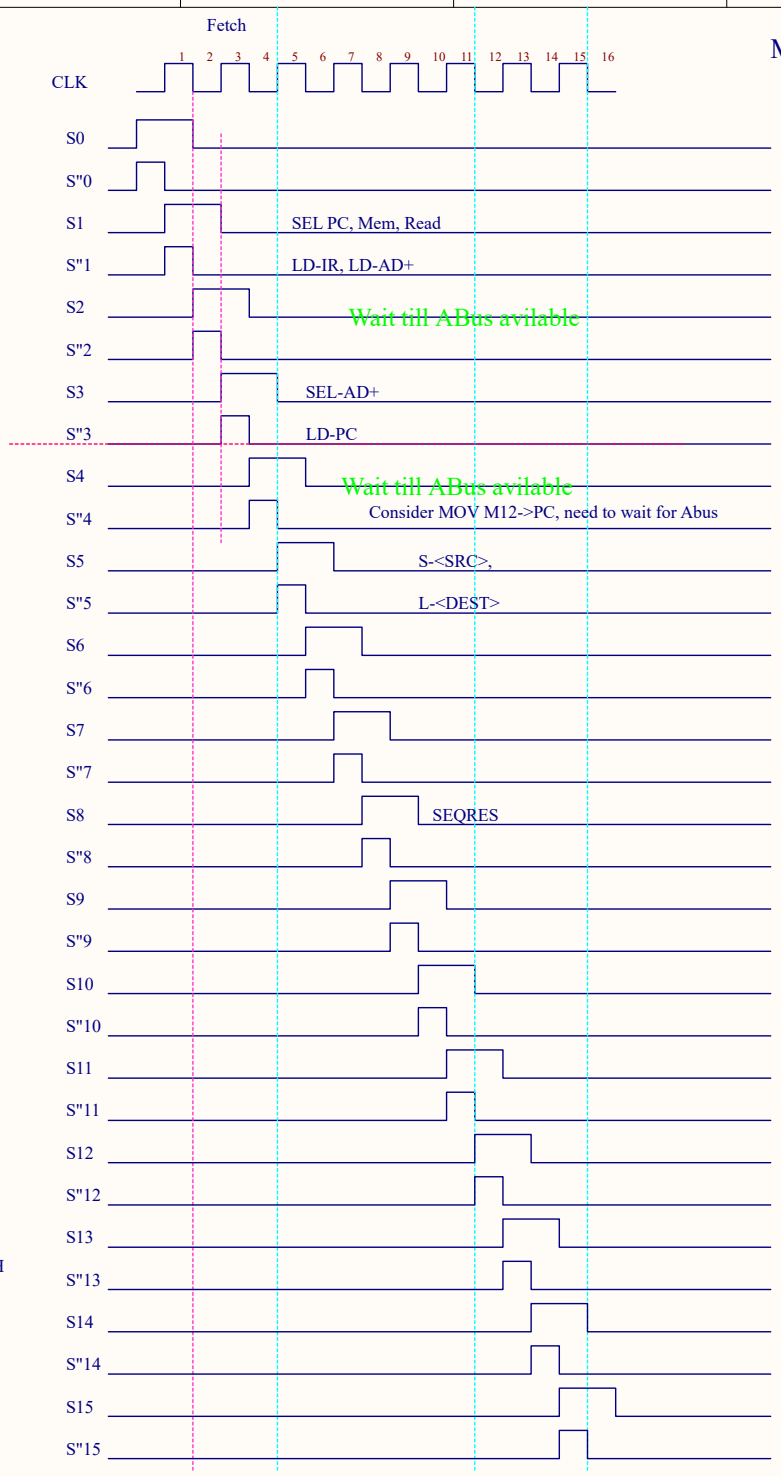
2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-LDI(R).SchDoc		Drawn By:

Sixteen stage state machine

MOV Timing



Fetch

Proposed Update 1/1/20

NB SEQRES timing

MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

SRC	DEST	Temp Dest
A=000	A=000	A=000
B=001	B=001	B =100
C=010	C=010	C=001
M=011	MH=011	MH=101
nc=100	ML=100	ML=010
PC+=101	PC+=101	AD+=101
PC=110	PC=110	PC=100
NULL=111	nc=111	nc=111

Problem c AD+, MH

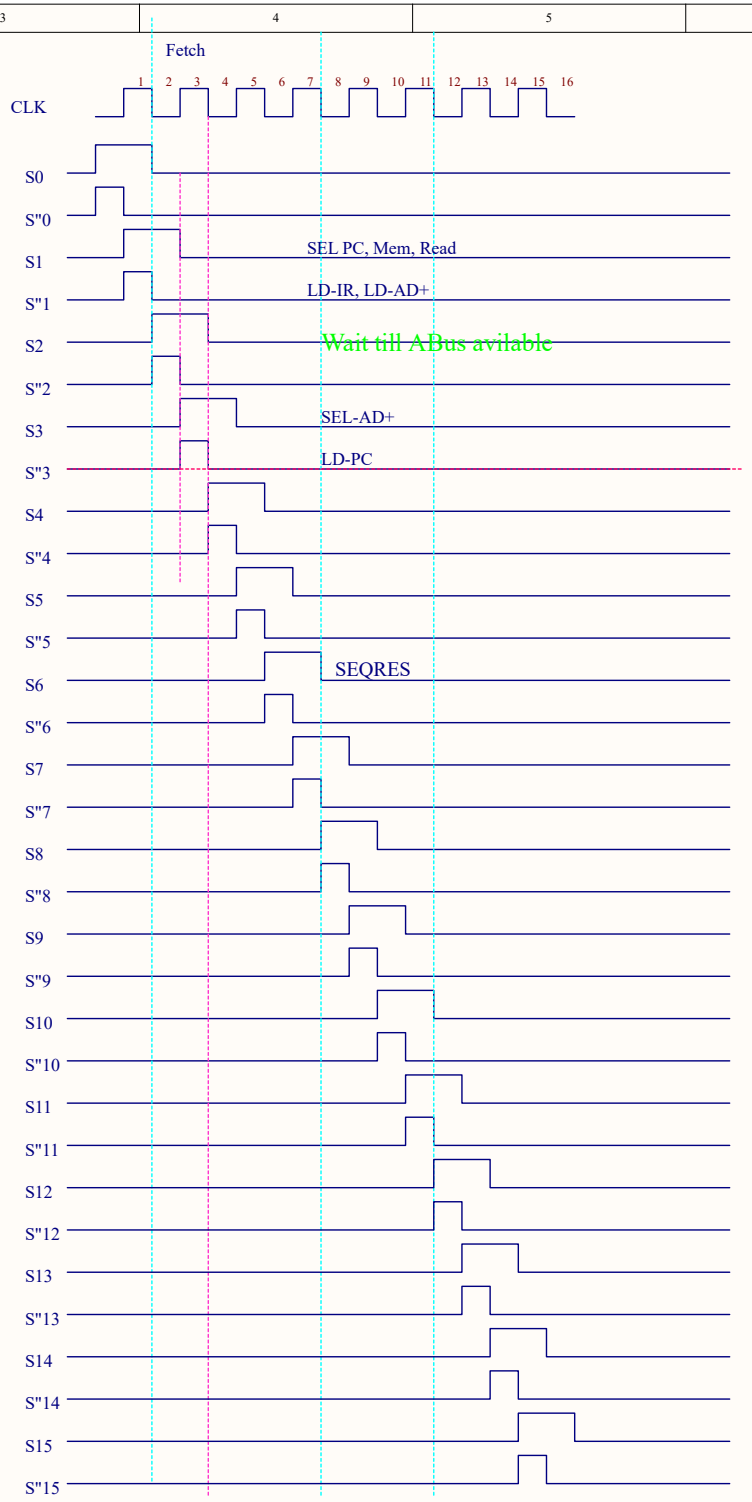
BRANCH

2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

Title: MOV Timing		
Size: A3	Number:	Revision:
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-MOV.SchDoc		Drawn By:

Sixteen stage state machine



MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

NOP

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

ALU Fn		DES
0000 = NOP	1000 = ADDAB	A=00
0001= RESET	1001 = A&B	B=01
0010 = HALT	1010 = NOTA	C=02
0011= WAIT0	1011 = INCB	
	1100 = RORA	
	1101 = ROLB	

BRANCH

2/4/2 instructions

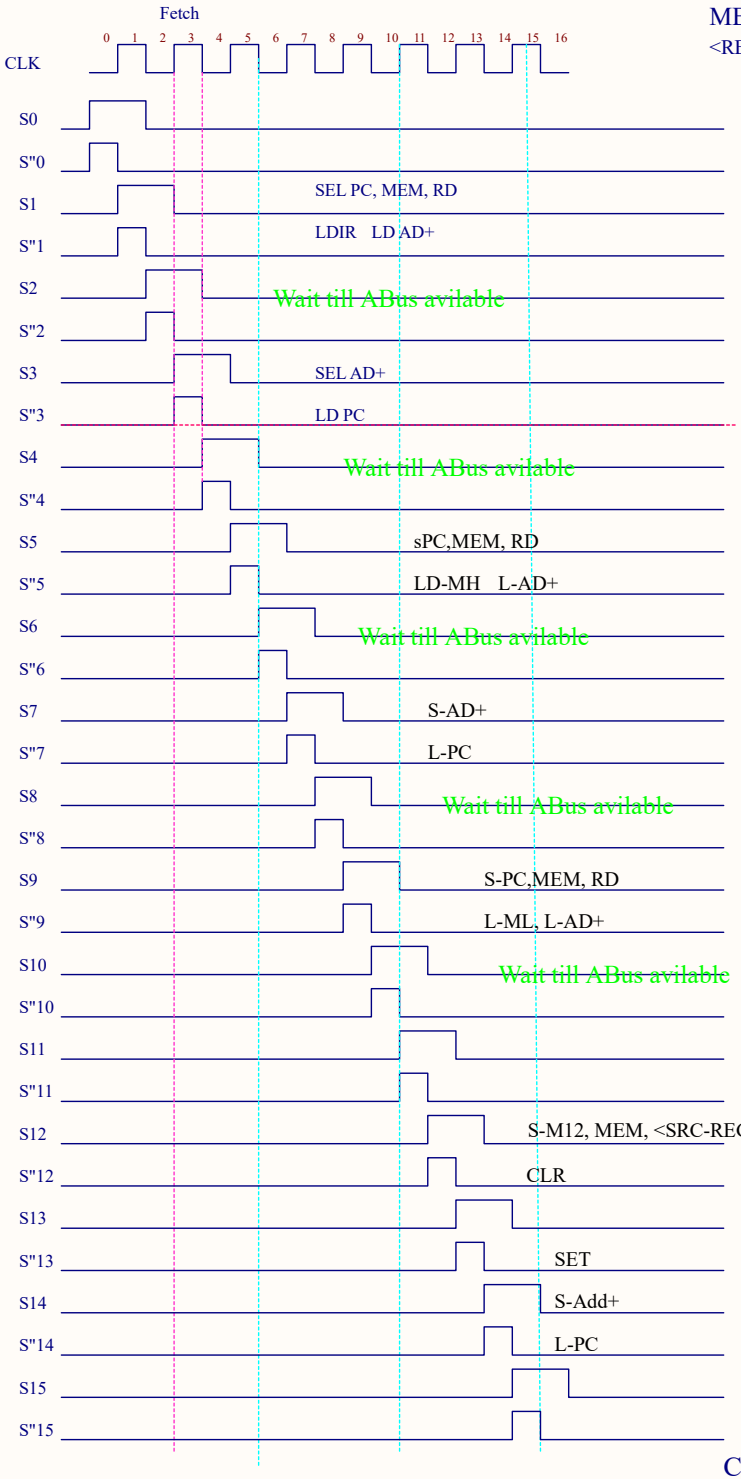
IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

0000 = BRZ	0006= BROVF
0001= BRP	0007= BRNOVF
0002= BRN	0008= BRA
0003= BRNZ	
0004= BRNP	
0005= BRNN	

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-NOP.SchDoc		Drawn By:

STA<REG>

Sixteen stage state machine



MEM

2/3/3

1	0	S	S	S	D	D	D

SRC	DEST	Temp
000 = A	000 = A	000 = A
001 = B	001 = B	100 = B
010 = C	010 = C	001 = C
011 = MMI	011 = nul	
100 = MMA	100 = MMA	010 = MMA

NB If DEST is MMA, then must be RAM
If SRC is MMI (Immediate) then can be ROM or RAM
If SRC is MMA (Absolute), can be ROM or RAM

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
2	2	S	S	S	D	D	D

MEM write
<REG> -> MEM-ABS

STA<REG>

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

Fetch

Load M12

Update 1/1/20

BRANCH

2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

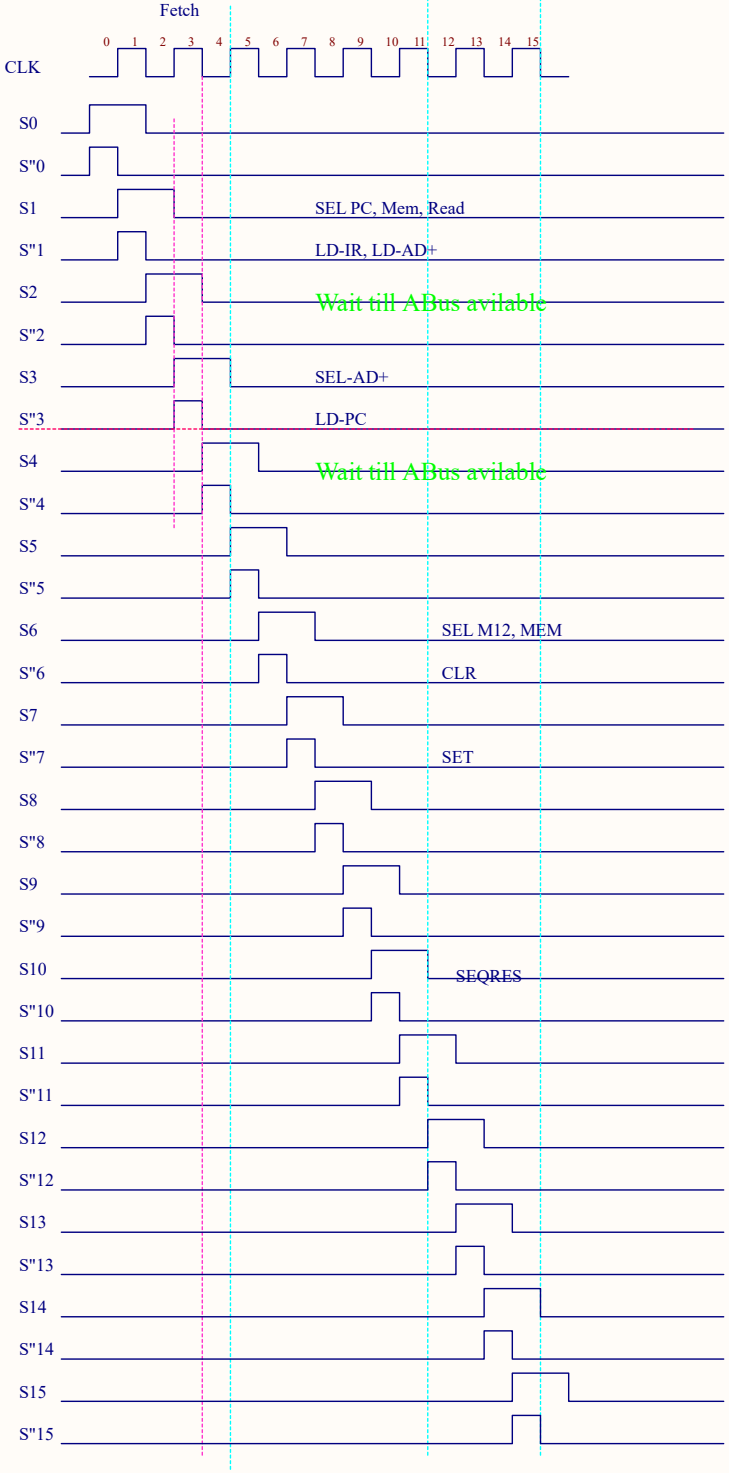
STA<REG>

Complete SQ Cycle

Title	MEM write		
Size A3	Number		Revision
Date: 10/02/2024		Sheet of	
File: C:\Users\..\Timing-STA(Write).SchDoc		Drawn By:	

STD<R> Store Direct

Sixteen stage state machine



MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

SRC	DEST	Temp
000 = A	000 = A	000 = A
001 = B	001 = B	100 = B
010 = C	010 = C	001 = C
011 = MMI	011 = nul	
100 = MMA	100 = MMA	010 = MMA
101 = MMD	101 = MMD	
111 = nul	111 = nul	

NB If DEST is MMA, then must be RAM
If SRC is MMI (Immediate) then can be ROM or RAM
If SRC is MMA (Absolute), can be ROM or RAM
DIRECT modes are LDD<R> & STD<R>
DIRECT modes apply preloaded M12 as SRC or DEST addresses

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

SRC	DEST	Temp Dest
A=000	A=000	A=000
B=001	B=001	B =100
C=010	C=010	C=001
M=011	MH=011	MH=101
nc=100	ML=100	ML=010
PC+=101	PC+=101	AD+=101
PC=110	PC=110	PC=100
NULL=111	nc=111	nc=111

Problem c AD+, MH

STD<R> Store Direct

Store REG into RAM at location held in Mem Addr Reg MR12

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

ALU Fn		DES
0000 = NOP	1000 = ADDAB	A=00
0001= RESET	1001 = A&B	B=01
0010 = HALT	1010 = NOTA	C=02
0011= WAIT0	1011 = INCB	
	1100 = RORA	
	1101 = ROLB	

BRANCH

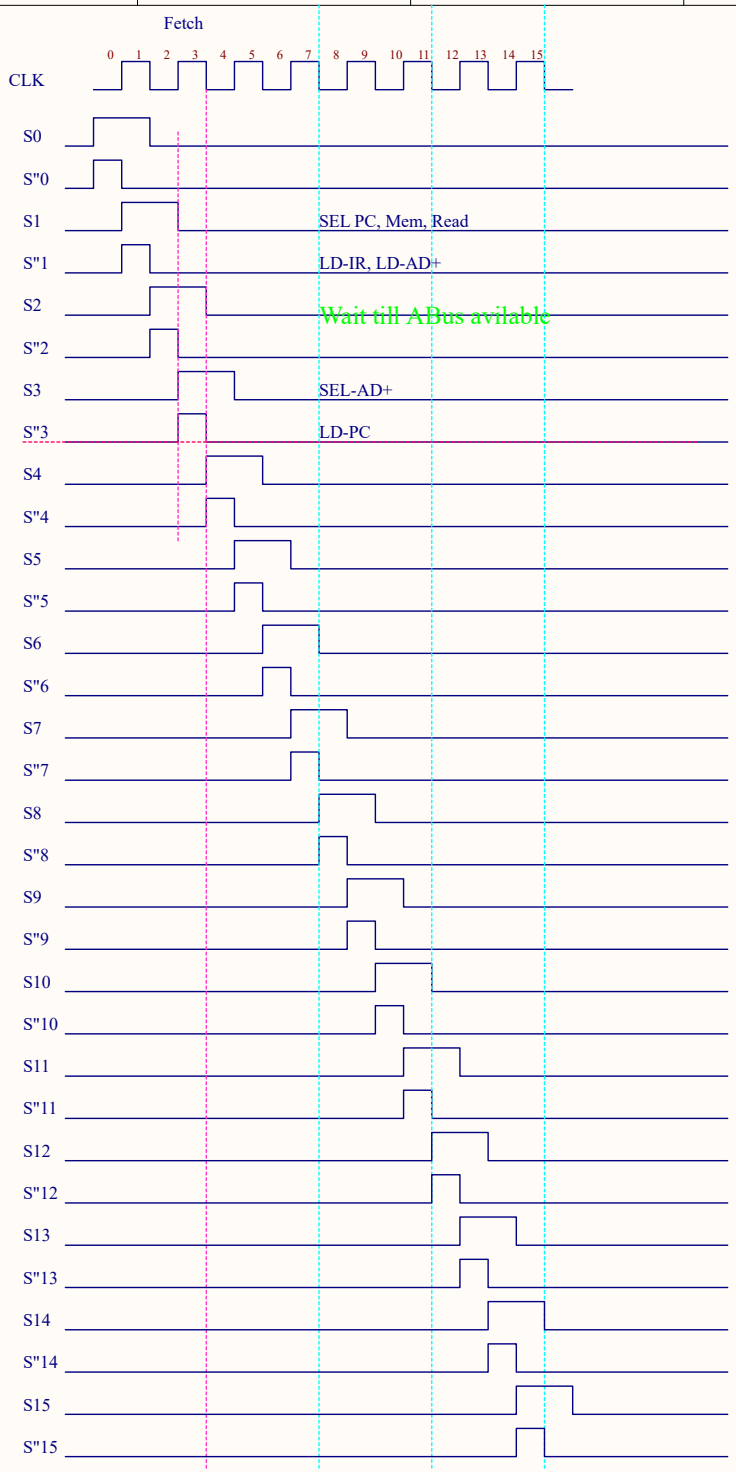
2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

0000 = BRZ	0006= BROVF
0001= BRP	0007= BRNOVF
0002= BRN	0008= BRA
0003= BRNZ	
0004= BRNP	
0005= BRNN	

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-STD(Write).SchDoc		Drawn By:

Sixteen stage state machine



MEM

2/3/3 instructions

IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
1	0	S	S	S	D	D	D

SRC	DEST	Temp
000 = A	000 = A	000 = A
001 = B	001 = B	100 = B
010 = C	010 = C	001 = C
011 = MMI	011 = nul	
100 = MMA	100 = MMA	010 = MMA
111 = nul		

NB If DEST is MMA, then must be RAM
If SRC is MMI (Immediate) then can be ROM or RAM
If SRC is MMA (Absolute), can be ROM or RAM

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

ALU Fn

0000 = NOP
0001= RESET
0010 = HALT
0011= WAIT0
1000 = ADDAB
1001 = A&B
1010 = NOTA
1011 = INCB
1100 = RORA
1101 = ROLB

DES

A=00
B=01
C=02

MOV

2/3/3 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
1	1	S	S	S	D	D	D

SRC	DEST	Temp Dest
A=000	A=000	A=000
B=001	B=001	B =100
C=010	C=010	C=001
M=011	MH=011	MH=101
nc=100	ML=100	ML=010
PC+=101	PC+=101	AD+=101
PC=110	PC=110	PC=100
NULL=111	nc=111	nc=111

Problem c AD+, MH

BRANCH

2/4/2 instructions

IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1
0	1	B	B	B	B	x	x

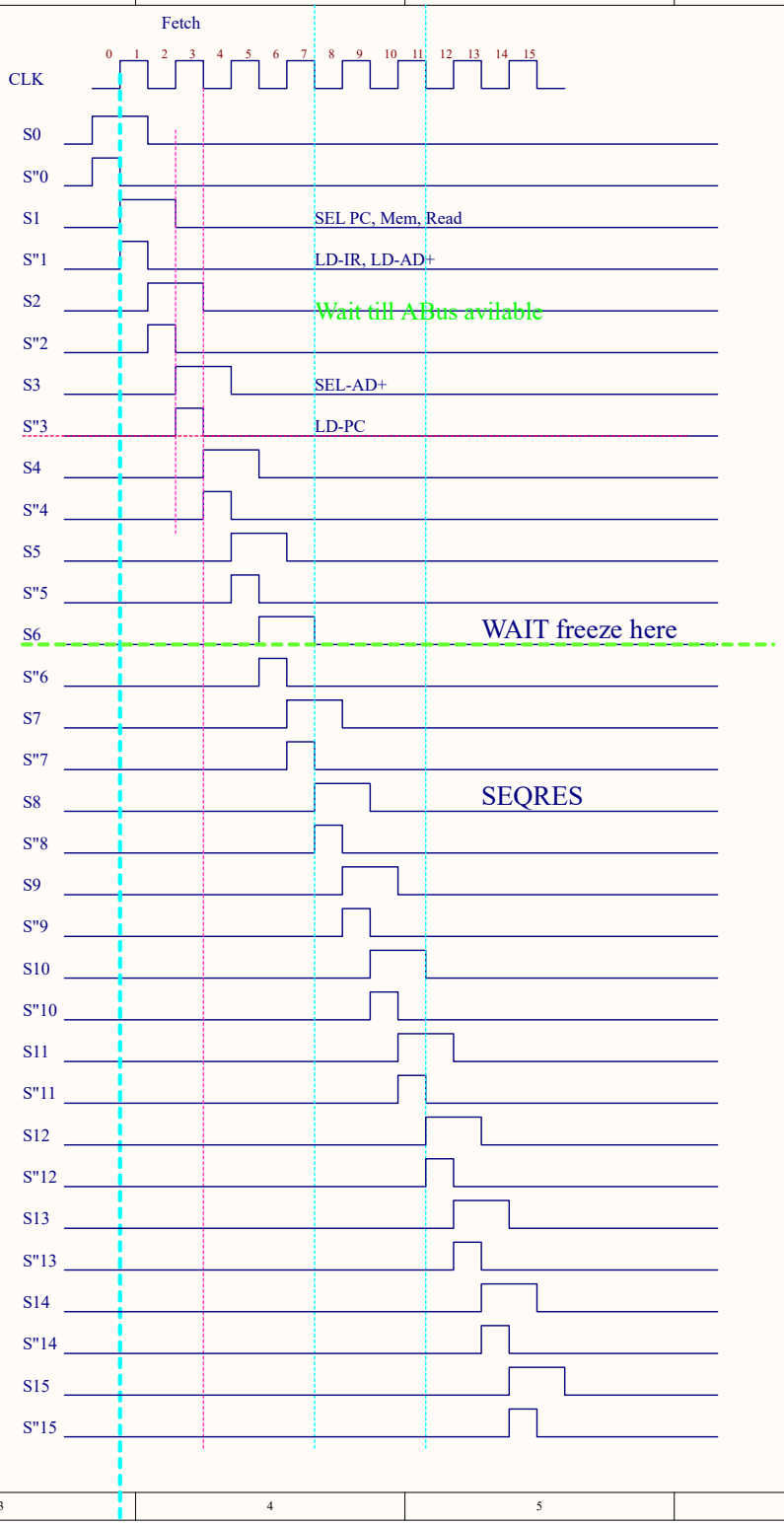
0000 = BRZ
0001= BRP
0002= BRN
0003= BRNZ
0004= BRNP
0005= BRNN
0006= BROVF
0007= BRNOVF
0008= BRA

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-template.SchDoc		Drawn By:

WAIT

Sixteen stage state machine

WAIT happens on the 0->1 edge of S1,
as soon as IR is loaded.
WAITING flag is latched and Wait-Block is latched.
WAITING causes CLKSRC motor to freeze.
Halt will also freeze motor.
Waiting is released by EndWait,
which will allow Clk propagation.
And motor to run.
The interrupted Fetch will complete, and
Wait-Block is released at S1 of next cycle.



WAIT

ALU

2/4/2 instructions

IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2
0	0	S/A	A	A	A	D	D

ALU Fn		DES
0000 = NOP	1000 = ADDAB	A=00
0001= RESET	1001 = A&B	B=01
0010 = HALT	1010 = NOTA	C=02
0011= WAIT0	1011 = INCB	
	1100 = RORA	
	1101 = ROLB	

Title		
Size A3	Number	Revision
Date: 10/02/2024		Sheet of
File: C:\Users\..\Timing-Wait.SchDoc		Drawn By: